

04-24-01
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant: Shen
Serial No.: 09/407,204
Filed: September 28, 1999

Examiner: Nitin Parekh
Group Art Unit: 2811
Docket: 8688.128US01

Title: SEMICONDUCTOR CHIP MODULE

CERTIFICATE UNDER 37 CFR 1.10

'Express Mail' mailing label number: EL 8155523062 US

Date of Deposit: April 23, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner of Patents and Trademarks, Washington, D.C. 20231.

By: Yolanda Gray

BOX FEE AMENDMENT
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal Sheet in duplicate containing Certificate of Mailing
- ☒ Amendment
- ☒ Small entity status has been previously established
- ☒ Request for Extension of Time for one (1) month(s) and fee of \$110.00
- ☒ Check(s) in the amount of \$110.00 for One (1) month extension of time
- ☒ Return postcard

Please consider this a PETITION FOR EXTENSION OF TIME for a sufficient number of months to enter these papers, if appropriate. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
P.O. Box 2903, Minneapolis, MN 55402-0903
612.332.5300

By: Michael D. Schumann
Name: Michael D. Schumann
Reg. No.: 30,422
MDS/VW/rmzc





09/407,204

PATENT

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By: Yolanda Gray
Name:

AMENDMENT UNDER 37 C.F.R. §1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated December 22, 2000, please amend this application as follows:

In the Claims

04/30/2001 AJOHNS01 00000001 Please add claims 20-21 as follows:

01 FC 103

18.00 CH 20. (New)

A semiconductor chip module comprising:

a chip-mounting member having opposite first and second surfaces,
a set of first circuit traces, a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces, and a set of second circuit traces accessible from the other one of said first and second surfaces opposite to said first circuit traces and connected to said plated through holes;